IN THE CLAIMS

1-18. (Canceled)

19. (Previously Presented) A method for measuring a voltage at an internal node of an integrated circuit, the method comprising:

coupling a pass circuit between the internal node and a pin of the integrated circuit;

using a reset circuit to activate the pass circuit; and

driving the pass circuit to pass the voltage from the internal node to the pin.

20. (Previously Presented) The method of claim 19, further comprising using a pass control circuit to drive the pass circuit.

21. (Previously Presented) The method of claim 20, further comprising using the pass control circuit to provide at least one output signal to selectively drive the pass circuit to pass a voltage from the internal node to the pin, thereby allowing the voltage at the internal node to be read after the integrated circuit is packaged.

22. (Previously Presented) The method of claim 20, wherein the pass control circuit comprises an n-channel MOS transistor having a drain coupled to the internal node, the n-channel MOS transistor configured to, when turned on, pass the voltage at the internal node to a source of the n-channel MOS transistor and to the pass circuit.

23. (Previously Presented) The method of claim 19, further comprising providing an oscillating control signal to the pass circuit.

24. (Previously Presented) The method of claim 23, further comprising using a ring oscillator to provide the oscillating control signal to the pass circuit.

25. (Previously Presented) The method of claim 19, further comprising using a pass control circuit to apply a desired voltage to the internal node, thereby forcing the voltage at the internal node to the desired voltage.

26. (Previously Presented) The method of claim 19, wherein the pass circuit comprises:

a pass gate having first, second, and third terminals, the first terminal coupled to a pass control circuit, the second terminal coupled to the internal node, the third terminal coupled to the pin; and

a capacitor coupled between the first terminal of the pass gate and the pass control circuit such that a voltage at the first terminal of the pass gate is driven to cause a voltage at the second terminal voltage to be passed to the third terminal for reading the voltage at the internal node.

27. (Previously Presented) The method of claim 26, wherein the pass gate comprises an n-channel MOS transistor.

28. (Previously Presented) A method for forcing a voltage at an internal node of an integrated circuit to a desired level, the method comprising:

coupling a pass circuit between the internal node and a pin of the integrated circuit;

applying a voltage of the desired level to the pin;

using a reset circuit to activate the pass circuit; and

driving the pass circuit to pass the applied voltage from the pin to the internal node, thereby forcing the voltage at the internal node to the desired level.

29. (Previously Presented) The method of claim 28, further comprising using a pass control circuit to drive the pass circuit.

30. (Previously Presented) The method of claim 28, wherein the pass control circuit comprises an n-channel MOS transistor having a drain coupled to the internal node, the n-

channel MOS transistor configured to, when turned on, pass the voltage at the internal node to a source of the n-channel MOS transistor and to the pass circuit.

31. (Previously Presented) The method of claim 28, further comprising providing an oscillating control signal to the pass circuit.

32. (Previously Presented) The method of claim 31, further comprising using a ring oscillator to provide the oscillating control signal to the pass circuit.

33. (Previously Presented) The method of claim 28, wherein the pass circuit comprises:

a pass gate having first, second, and third terminals, the first terminal coupled to a pass control circuit, the second terminal coupled to the internal node, the third terminal coupled to the pin; and

a capacitor coupled between the first terminal of the pass gate and the pass control circuit such that a voltage at the first terminal of the pass gate is driven to cause a voltage at the second terminal voltage to be passed to the third terminal for reading the voltage at the internal node.

34. (Previously Presented) The method of claim 33, wherein the pass gate comprises an n-channel MOS transistor.

35. (Previously Presented) A method comprising:

receiving a read signal;

coupling a pass circuit between an internal node and a pin of an integrated circuit;

resetting the pass circuit with a reset circuit based on a first state of the read signal; and

passing the voltage from the internal node to the pin based on a second state of the read signal.

36. (Previously Presented) The method of claim 35, wherein passing the voltage from the internal node includes driving a control node connected to the pass circuit to a first voltage based on the second state of the read signal.

37. (Previously Presented) The method of claim 36, wherein driving includes passing an oscillating signal to the pass circuit.

38. (Previously Presented) The method of claim 36, wherein resetting the pass circuit includes driving the control node to a second voltage based on the first state of the read signal.

39. (Previously Presented) The method of claim 38, wherein resetting the pass circuit includes driving the control node to ground.

40. (Previously Presented) A method comprising:
receiving a read signal;
coupling a pass circuit between an internal node and a pin of an integrated circuit;
applying an applied voltage to the pin;
resetting the pass circuit with a reset circuit based on a first state of the read signal; and
passing the applied voltage from the pin to the internal node based a second state of the read signal.

41. (Previously Presented) The method of claim 40, wherein passing the applied voltage from the pin includes driving a control node connected to the pass circuit to a first voltage based on the second state of the read signal.

42. (Previously Presented) The method of claim 41, wherein driving includes passing an oscillating signal to the pass circuit.

43. (Previously Presented) The method of claim 41, wherein resetting the pass circuit includes driving the control node to a second voltage based on the first state of the read signal.

44. (Previously Presented) The method of claim 43, wherein resetting the pass circuit includes driving the control node to ground.

45. (Previously Presented) A method comprising:

receiving a read signal;

passing a voltage between an internal node and an access pin based on a first signal level of the read signal; and

isolating the access pin from the internal node based on a second signal level of the read signal.

46. (Previously Presented) The method of claim 45, wherein passing a voltage includes pulling a control voltage of a control node to a first voltage level based on the first signal level of the read signal.

47. (Previously Presented) The method of claim 46, wherein isolating the access pin includes pulling a control voltage of a control node to a second voltage level based on the second signal level of the read signal.

48. (Previously Presented) The method of claim 45, wherein passing a voltage includes:

activating a control device connecting between the internal node and a pass node; and

activating a pass device connecting between the pass node and the access pin.

49. (Previously Presented) The method of claim 48, wherein isolating the access pin includes deactivating the pass device.

50. (Previously Presented) The method of claim 49, wherein isolating the access pin includes deactivating the control device.

51. (Previously Presented) The method of claim 50, wherein isolating the access pin includes connecting the pass node to ground.

52. (Previously Presented) The method of claim 45, wherein isolating the access pin includes disabling a pass circuit connected between the access pin and the internal node.

53. (Previously Presented) The method of claim 45, wherein isolating the access pin includes disconnecting a pass circuit connected to the access pin from a pass control circuit connected to the internal node.

54. (Previously Presented) The method of claim 45, wherein isolating the access pin includes disconnecting a first terminal of a pass device connected to the access pin from a second terminal of the pass device connected to the internal node.

55. (Previously Presented) The method of claim 45, wherein isolating the access pin includes cutting off a conduction channel between a source of a pass transistor connected to the access pin and a drain of the pass transistor.

56. (Previously Presented) A method comprising:

receiving a read signal;

passing an internal voltage from an internal node to an access pin based on a first signal level of the read signal; and

isolating the access pin from the internal node based on a second signal level of the read signal.

57. (Previously Presented) The method of claim 56, wherein passing an internal voltage includes:

passing the internal voltage to a pass node; and

passing the internal voltage from the pass node to the access pin.

58. (Previously Presented) The method of claim 57, wherein:

passing the internal voltage to a pass node is performed by a pass control circuit connecting between the internal node and the pass node; and

passing the internal voltage from the pass node to the access is performed by a pass circuit connecting between the pass node and the access pin.

59. (Previously Presented) The method of claim 57, wherein isolating the access pin includes pulling a voltage of the pass node to ground.

60. (Previously Presented) The method of claim 56, wherein passing an internal voltage includes:

activating a control device connecting between the internal node and a pass node; and

activating a pass device connecting between the pass node and the access pin.

61. (Previously Presented) The method of claim 60, wherein isolating the access pin includes deactivating the pass device.

62. (Previously Presented) The method of claim 61, wherein isolating the access pin includes deactivating the control device.

63. (Previously Presented) The method of claim 62, wherein isolating the access pin includes connecting the pass node to ground.

64. (Previously Presented) A method comprising:

receiving a read signal;

passing a pin voltage from an access pin to an internal node based on a first signal level of the read signal; and

isolating the access pin from the internal node based on a second signal level of the read signal.

65. (Previously Presented) The method of claim 64, wherein passing a pin voltage includes:

turning on a control transistor connecting between the internal node and a pass node; and

turning on a pass transistor connecting between the pass node and the access pin.

66. (Previously Presented) The method of claim 65, wherein isolating the access pin includes turning off the pass transistor.

67. (Previously Presented) The method of claim 66, wherein isolating the access pin includes turning off the control transistor.

68. (Previously Presented) The method of claim 67, wherein isolating the access pin includes connecting the pass node to ground.

69. (Previously Presented) A method comprising:

receiving a read signal;

activating a control device during a first signal level of the read signal to pass a voltage between an internal node inside a memory device and a pass node inside the memory device;

activating a pass device during the first signal level of the read signal to pass the voltage between the pass node and an input/output pin of the memory device;

deactivating a reset circuit during the first signal level of the read signal to isolate the pass node from ground;

deactivating the control device during a second signal level of the read signal;

deactivating the pass device during the second signal level of the read signal; and

activating the reset circuit during the second signal level of the read signal to connect the pass node to ground.

70. (Previously Presented) The method of claim 69, wherein activating a control device during a first signal level of the read signal to pass a voltage between an internal node inside a memory device and a pass node inside the memory device includes:

passing an internal voltage from the internal node to the pass node.

71. (Previously Presented) The method of claim 70, wherein activating a pass device during the first signal level of the read signal to pass the voltage between the pass node and an input/output pin of the memory device includes:

passing the internal voltage from the pass node to the input/output pin.

72. (Previously Presented) The method of claim 71, wherein activating a control device during a first signal level of the read signal to pass a voltage between an internal node inside a memory device and a pass node inside the memory device includes:

passing an applied voltage from the pass node to the internal node.

73. (Previously Presented) The method of claim 72, wherein activating a pass device during the first signal level of the read signal to pass the voltage between the pass node and an input/output pin of the memory device includes:

passing the applied voltage from the input/output pin to the pass node.